PATENT
Docket 21MMC-10

REMARKS

Reconsideration of the above identified application is respectfully requested.

The specification has been amended at para. 5 to correct a spelling error, and at para. 44 to conform with para. 22.

On 12 March 2003, the undersigned attorney conducted a phone interview with examiner Patel to briefly discuss the rejections of record. Although no agreement was reached, this amendment is being presented consistent with the interview for further consideration.

In particular, it is noted that reference "AJ" in the form PTO-1449 lacks initialing by the examiner. Accordingly, the form should be initialed by the examiner to confirm due consideration of the cited reference, with a fully initialed copy of the form provided with the next office action.

Applicants traverse the restriction requirement; and confirm the provisional election of Group I, claims 1-27.

The examiner's contention that the product as claimed could be made by forming the well and ledge "before laminating together" is not a difference at all, let alone a material difference. Method claim 28 does not require that the well and ledge be formed before or after the laminating feature; both before and after formation are well within the scope of this broad process claim.

The examiner's additional contention that the bottom plate "can be glued to the board instead of lamination" is also not a difference at all, let alone a material difference. Claim 28 broadly covers lamination by any means, including the "glued" example proposed by the examiner.

Furthermore, it is also noted that the "separate [search] status" proffered by the examiner in para. 3 of the office action is not confirmed by the actual search classes listed in the form PTO-892; and, in fact, class 29/832 is listed for

reference K, which class conforms to the Group II invention proffered by the examiner.

Finally, MPEP 821.04 suggests that process claims, like claim 28, be presented in the same application as the product claims, and preferably made dependent therefrom. And, upon allowance of the product claim, the process claim must be rejoined.

Accordingly, withdrawal of the restriction requirement is warranted and is requested.

Applicants traverse the rejection of claims 1-27 under Section 103(a) over references Thaler et al and Yoshikawa et al ('165).

Applicants also traverse all of the examiner's contentions as being inaccurate interpretations of the applied references, and failing to meet the specificity requirements of the MPEP.

MPEP 706.02(j) provides the basic requirements which must be provided by the examiner in establishing prima facie obviousness under 35 U.S.C. 103. Four steps are required of the examiner including: (1) relevant teachings; (2) claim differences; (3) proposed modification of the reference(s) to arrive at the claimed subject matter; and (4) an explanation the proposed modification would have been obvious under Section 103.

The MPEP also requires a showing by the examiner of three basic criteria to establish a prima facie rejection including: first, evidence for the suggestion or modification for modifying or combining references; second, a reasonable expectation of success; and finally, the reference(s) must teach or suggest all the claim limitations, and cannot be based on applicant's own disclosure.

Citing Ex Parte Clapp, the MPEP places the burden of proof on the examiner to provide evidence to support the conclusion of obviousness either from the references which

must expressly or impliedly suggest the claimed invention, or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.

It is the examiner who must meet this initial burden by applying specific evidence; and clearly the examiner has not met this burden with the unsupported "therefore" conclusions of obviousness, which fail to meet the stringent "legal motivation" requirements of MPEP ch. 2100.

The MPEP also requires the examiner to consider the claims and the references in the whole, including the problems being solved. The examiner has failed to show how the two references have any nexus to each other in the first place, or why one skilled in the art would have wanted to combine the disparate teachings thereof for any reason.

Without Applicants' claims as the guide, one skilled in the art would not know what to select from these references and what to disregard. The examiner's combination of these references "in order to amplify input/output signal" has no technical relevance with these references or the problems being solved therein, or, more importantly, the specific problems being solved by the Applicants. And, the contention does not meet the legal motivation requirement.

Fundamentally, however, claim 1 recites that the chip 24 is electrically connected to the printed circuit boards 18 and electrically bonded to the bottom conductor plate 20. This configuration has many, many benefits repeatedly emphasized in the specification, including RF grounding and shielding for the RF chip itself.

Thaler discloses multiple embodiments sharing common features including the IC components 30,72,108 merely "seated" on the metal base plates 12,72,108. Those IC's have terminals 32,74,110 which provide the electrical connections to the conductive layers 20 etc. by the wires 34 etc.

PATENT
Docket 21MMC-10

The examiner's contention of "electrical connection of the component, see figure 3, column 3, line 50-55)" merely recognizes that the wires 76 in the second embodiment of Thaler provide the connection in a quite conventional manner. See for example the wires 44 in Applicants' figure 4.

However, claim 1 recites more. Claim 1 recites that the chip 24 is "electrically bonded atop said plate," yet no such electrical bonding appears disclosed in Thaler, instead the wires 76 identified by the examiner provide a different electrical connection.

The examiner's combination of Yoshikawa '165 fails to remedy this fundamental shortcoming of Thaler, and overlooks how the chip 1 in Yoshikawa '165 is mounted to the substrate 2d by the solder 5. Yet, that substrate 2d is "composed of ceramic material," which is a dielectric, not metal as found in Thaler. If anything, Yoshikawa '165 would appear to teach away from the examiner's selective combination thereof with Thaler because there can be no electrical bond or path from the chip 1 to the ceramic substrate 2d.

For these exemplary reasons alone, it is not seen how a prima facie showing under Section 103 has been made from references Thaler and Yoshikawa '165 for any of claims 1-27 being rejected, with claims 2-27 providing additional details for which the examiner's contentions are unfounded.

In particular, claims 2 and 8 recite additional features of the electrical connection between the chip and bottom plate for the many advantages disclosed in the specification. As discussed during the interview, and as a courtesy to the examiner in better distinguishing over the applied references for promoting early termination of prosecution, claim 1 is being amended to now include the features previously recited in claims 2 and 8.

These include the metalized base 26 of the chip 24 which provides an integral ground for the chip and the printed

circuit boards.

The examiner's contention at the bottom of page 4 regarding claim 2 is not supported by the applied references. None of "figures 1, 2 and 3" of Thaler, or its other figures disclose or suggest the "metalized base" feature of claim 2, now embodied in claim 1, and the examiner has not shown otherwise. Thaler merely discloses that the IC component 30 is "seated," and that the electrical connections are provided by the wires 34,76,112.

The examiner's contentions regarding claim 8 are presented at page 5 of the office action, and are also unsupported by the applied references. "Column 1, line 60 to column 2, line 26" of Thaler clearly does not support the examiner's contention. This section of Thaler describes the base plate 12 and the body 16.

The IC component 30 is not introduced until col. 2, line 28, which clearly states that: "In each of the openings 28 and seated on the surface 14 of the base plate 12 is an electronic circuit component 30." There is no disclosure in Thaler that such "seating" is an electrical connection, nor that any ground is provided thereat.

In view of these fundamental features now recited in amended claim 1, withdrawal of the entire rejection of all claims over the applied references is warranted.

Since the features of claims 2 and 8 have been moved to claim 1, claim 2 has been amended to include features previously recited in claims 5 and 6. This includes the dielectric substrate 36 and integral metal layer 38 for the boards 18, with the metal layers defining the printed circuits for operating the chip, as well as including independent portions for providing radio frequency grounding and EMI shielding for the considerable benefits presented in the specification.

The examiner's reference at page 5 of the office action

to Thaler and Yoshikawa '165 for claims 3-6 fails to show any analogous printed circuits in Thaler for operating the IC component 30, or that the circuits 21,23 of Yoshikawa '165 could or would be combined in Thaler. The examiner's use of "column 2, line 50-55" for claim 6 overlooks the express recitation in claim 6, and the express teaching of Thaler. Thaler merely teaches that: "some of the electrically conductive layers 18 may be used as ground planes for the electronic circuit components 30." Yet this is not relevant to claim 6 as now found in claim 2. Amended claim 2 recites that the metal layers include independent portions not part of the printed circuits as disclosed at para. 42 for the RF grounding benefit. Where is this taught or suggested in the applied references?

Claim 3 has been amended to conform with claim 2; and the examiner has failed to show in the applied references any analogous impedance matching circuits.

Claim 4 recites that the top board 18a includes electronic components 34 for the impedance matching circuits. No such components are found in Thaler, and the circuits 21,23 in Yoshikawa '165 are differently configured and located in the intermediate substrates.

Since the features of claim 5 have been moved to claim 2, claim 5 has been amended to newly recite that the independent grounding portions are distributed between the printed circuits for the advantages disclosed in the specification, beginning at para. 43. Neither reference discloses or suggests such features, and lack detailed disclosure of the form of electrical paths in the substrates.

Since the features of claim 6 have been moved to claim 2, claim 6 has been amended to newly recite the matching configuration of the bottom plate 20 and the laminated boards 18 for the advantages presented in paras. 27 and 31, including the large heat sink and RF grounding.

Neither reference is so configured, with Thaler not teaching an RF grounding plate; and Yoshikawa '165 having a large ceramic substrate 2d and a small heat dissipating electrode 15.

Claim 7 recites interconnections between the layers which distinguishes over the examiner's contentions at page 5 of the office action which fail to afford due weight to the RF grounding feature of the bottom plate.

Since the features of claim 8 have been moved to claim 1, claim 8 has been amended to newly recite the dedicated vertical terminals for electric grounding of the metal layers for the benefits disclosed at para. 46. Neither Thaler nor Yoshikawa '165 appear to disclose any dedicated vertical terminals for such grounding.

Claim 9 recites a module wherein the boards further comprise a bottom board 18c projecting into the well 22 to define a ledge 42 surrounding the chip 24, and the chip top terminals 28 are electrically joined to the printed circuits atop the ledge. The examiner's use of Thaler and Yoshikawa '165 fails to afford due weight to the RF grounding feature between the chip and bottom plate.

Claim 10 recites a module wherein the chip top terminals 28 are electrically joined to the ledge 42 by respective wires 44 having length, diameter, and material property for effecting a predetermined inductance in the printed circuits.

The examiner has failed to show how the wires in Thaler and Yoshikawa '165 have any function in effecting desired inductance, let alone predetermined inductance for the benefits disclosed in the specification.

Claim 11 recites a module wherein the boards consist of three boards defining the well 22, with each of the boards defining a respective portion of the printed circuits. Both Thaler and Yoshikawa '165 disclose more than three layers, and therefore fail to disclose or suggest the three-board

configuration of claim 11 having the advantages presented in the specification.

Claim 12 recites a module wherein the well 22 includes a single chip 24 configured for single band radio frequency operation, and the bottom plate 20 includes five terminals 1-5 electrically insulated therefrom and electrically joined to the printed circuits for inputting and outputting a radio frequency signal through the chip with impedance matching to external circuits.

The examiner admits that both references fail to teach these features. The attempt by the examiner to use the "inherent" argument is without evidentiary or legal support, fails to afford any weight to the benefits of these features expressly contained in the specification, and is against the very teachings of Thaler and Yoshikawa '165. Note the multitude of terminal bumps 26 in figure 2 of Thaler. Note the six terminals in figure 2 of Yoshikawa '165.

Claim 12 does not merely recite the "required number of terminals" but fewer, in view of the synergy in combining the chip with its many terminals and the printed circuits, including its terminals.

The examiner's contention to modify Thaler to five terminals is not supported by either reference, and would render the configuration of Thaler inoperable for its intended purpose since, many, many more than "five" terminals are required in that reference.

Claim 13 recites a module wherein the well 22 includes a pair of the chips 24 configured for dual band radio frequency operation, and the bottom plate 20 includes corresponding sets of five terminals 1-10 electrically insulated therefrom and electrically joined to the printed circuits for inputting and outputting respective dual band radio frequency signals through the chips with impedance matching to external circuits.

The examiner has overlooked these features and the synergy and benefits disclosed in the specification. Neither reference discloses or suggests dual band configurations as recited in claim 13, and the examiner has not shown otherwise.

Claim 14 recites a module wherein the chip 24 comprises Gallium Arsenide Heterojunction Bipolar Transistors, and the bottom plate 20 underlies substantially all of the bottom board 18c.

The examiner's contentions fails to afford any weight to this claim, including the specific problems associated with RF chips such as the recited chip. And, the examiner's contention to combine "in order to have improved efficiency and overall performance of the amplifier system" is mere conjecture, and unsupported by the references, and is clearly not the legal motivation required by the MPEP.

Claim 15 recites a module further comprising a metal cover 46 enclosing the top board 18a and well 22 for providing shielding for electromagnetic interference. The examiner's reference to figure 1 of Yoshikawa '165 fails to meet the stringent requirements of the MPEP, and is clearly hindsight reconstruction without regard to the whole of the claim.

Claim 16 recites a module further comprising metal sidewalls 48 surrounding the laminated boards 18. Again, the examiner has failed to provide any legal motivation to combine Thaler and Yoshikawa '165 for any reason relevant to this claim.

Claim 17 recites a module wherein the metal cover 46, metal sidewalls 48, and metal bottom plate 20 are electrically interconnected, and substantially enclose the laminated boards 18 and radio frequency chip 24. Yet again, the examiner has failed to provide any legal motivation to combine Thaler and Yoshikawa '165 for any reason relevant to this claim.

Claim 18 recites a module further comprising a metal top plate 50 bonded to the top board 18a to hermetically close the

well 22 and chip 24 therein.

The examiner's grouping together of claims 15 and 18 is indicative of the failure to evaluate these claims in the whole; nor, has the examiner provided any legal motivation for any combination.

With respect to the metal elements recited in claims 15-18, the examiner has overlooked the express configuration of Thaler which has no such surrounding elements at all. Why add them in Thaler? What problem is being solved?

The features of Yoshikawa '165 cannot be combined for contrived reasons in hindsight, but the MPEP requires much more: it requires legal motivation, fundamentally lacking in the examiner's various rejections.

Claim 19 recites a module wherein the top plate is electrically grounded to the bottom plate 20 through the printed circuits.

Claim 20 recites a module wherein the boards further comprise a cover 18d electrically bonded to the top board 18a atop the well 22 to define a portion of the printed circuits.

The examiner admits that the references fail to disclose the features of claims 19 and 20; yet has provided no evidence to support the contention that "such grounding is known in the art for shielding the component."

Examiner argument is never evidence, and the lack of evidence relevant to these claims is conspicuous. The MPEP requires much more in rejecting claims, and the examiner has clearly failed to meet the evidentiary burden, and has failed to afford any weight to these claims and their benefits.

The examiner has grouped together claims 21-27, and therefore failed to meet the stringent requirements to examine each and every claim on its own merits. Indeed, the examiner's contention that "applicant is not disclosing any specific advantage of providing such cover with substrate" is clearly erroneous.

PATENT
Docket 21MMC-10

All claims 21-27 are well presented in the specification, including the "specific advantages" thereof, overlooked by the examiner in the rush to reject these claims.

The examiner's contention "to provide the combination ... with the component to accommodate the required component into the assembly" has no technical or logical merit, and is without evidentiary basis.

Claim 21 recites a module wherein the cover board 18d also includes a dielectric substrate 36 and a printed circuit layer 38, and the printed circuit layer thereof comprises an additional electronic component 34 for the impedance matching circuits. There is no teaching in Thaler and Yoshikawa '165 in this regard because they are not only different from each other, but different from this claim.

Clearly, the examiner has run out of parts in Thaler and Yoshikawa '165, and has chosen not to combine further references for the naked parts thereof. Selective combinations of references is not permitted by the MPEP, nor is the examiner's resort to "inherency" or "well known." The MPEP mandates evidence in rejecting claims, so that that evidence may be objectively evaluated under the stringent requirements of the MPEP.

Claim 22 recites a module 21 wherein the printed circuit layer 38 of the cover board 18d is disposed atop the substrate thereof. Neither Thaler nor Yoshikawa '165 have any teaching here.

Claim 23 recites a module 22 wherein the printed circuit layer 38 of the cover board 18d defines an inductor loop 34a. Again, neither Thaler nor Yoshikawa '165 have any relevance here. Note, however, that the examiner has already used circuits 21,23 in Yoshikawa '165, so why would it be obvious to introduce the inductor loop of claim 23 in either reference Thaler and Yoshikawa '165?

Claim 24 recites a module wherein the cover board 18d

further includes a bottom metal layer 38 covering the well 22 and radio frequency chip 24 therein. The examiner has failed to show any evidence in Thaler or Yoshikawa '165 relevant to this claim, or how or why they would have been modified for any reason relevant to this combination.

Claim 25 recites a module wherein the printed circuit layer 38 of the cover board 18d is disposed below the substrate thereof. Yet again, the examiner has provided no evidence relevant to this claim.

Claim 26 recites a module wherein the additional electronic component 34 is disposed inside the well 22 suspended below the bottom metal layer of the cover board. Nothing in Thaler or Yoshikawa '165 is relevant to this claim, and the examiner has not shown otherwise.

Claim 27 recites a module wherein the cover board 18d further includes a top metal layer 38 disposed atop the substrate thereof. This last product claim, too, is clearly not disclosed or suggested by Thaler and Yoshikawa '165, and the examiner has not shown otherwise.

The examiner's omnibus rejection of all twenty-seven product claims is indicative of the failure to afford due weight to each and every one of those claims, which claims are well described in the specification and provide corresponding advantages in solving the expressed problems in RF devices.

This technology is clearly sophisticated and esoteric, and the MPEP requires clear evidence in rejecting claims, especially for esoteric art.

Nevertheless, the examiner's cooperation in conducting the phone interview is appreciated. And, notwithstanding the typically broad interpretation of claims found in standard USPTO practice, the claims have been amended to further distinguish over the art of record.

Accordingly, withdrawal of the rejection of claims 1-27 under Section 103(a) over Thaler et al and Yoshikawa '165 et

PATENT
Docket 21MMC-10

al is warranted and is requested.

The additional references cited, but not applied, have been noted.

In accordance with the duty imposed by 37 CFR 1.104 and MPEP sections 707, 707.05, 707.07, and 707.07(g), the examiner is requested to reconsider all the art of record, including the additional references not applied, to ensure full compliance with the required thoroughness of examination.

In re Portola Packaging, Inc., 42 USPQ2d 1295 (Fed. Cir. 1997) emphasizes the importance of complying with this duty to ensure that all references of record have been fully considered by the examiner in the various combinations thereof. And, the Board of Appeals has further elaborated on the importance of this examiner duty in Ex parte Schricker, 56 USPQ2d 1723 (B.P.A.I. 2000).

Since the product claims should now be in condition for allowance, rejoinder of method claim 28 under MPEP 821.04 is now warranted. This claim has therefore been amended to better conform with claim 5 from which it depends.

In view of the above remarks, allowance of all claims 1-28 over the art of record is warranted and is requested.

Respectfully submitted,

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